IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Joseph P. Kerzman et al.

Serial No.: 08/789,025 Examiner: H. Jones

Filing Date: January 27, 1997 Group Art Unit: 2763

For: METHOD AND APPARATUS FOR EFFICIENTLY VIEWING A NUMBER OF SELECTED COMPONENTS USING A DATABASE EDITOR TOOL

Docket No.: 33012/184/101

TRANSMITTAL SHEET

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

CERTIFICATE UNDER 37 C.F.R. 1.8: I hereby certify that this correspondence and the documents described herein are being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Assistant Commissioner for Patents, Washington, D.C. 20231, on this 30th day of July, 2001

By John L. Rooney
John L. Rooney

We are transmitting herewith the attached:

[ ] Amendment

[ ] No additional fee required
[ ] The fee has been calculated as shown:

CLAIMS AS AMENDED							
	(3)	(4)	(5)	SMALL ENTITY		OTHER	
	REMAINING CLAIMS	HIGHEST PAID	EXTRA	RATE	ADD'L FEE	RATE	ADD'L FEE
TOTAL CLAIMS	-	=		x9=	$	x18=	$
INDEPEN-DENT CLAIMS	-	=		x39=	$	X78=	$
( ) FIRST MULTIPLE DEPENDENT CLAIM				+130=	$	+260 =	$
TOTAL				$		$	

[ ] A check in the amount of $_____ is enclosed.

[ ] Small entity status of this application under 37 C.F.R. 1.9 and 1.27 has been established by verified statement previously submitted.

[XXXX] Other: Appellant's Second Supplemental Brief Filed Under 37 CFR § 1.192 in Triplicate.

[XXXX] Please charge any deficiencies or credit any over payment in the enclosed fees to Deposit Account 14-0620.

By: John L. Rooney
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#B

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of	
Joseph P. Kerzman et al.	Examiner H. Jones
Serial No. 08/789,025	Group Art Unit 2763
Filing Date: 01/27/97	
For: METHOD AND APPARATUS FOR EFFICIENTLY VIEWING A NUMBER OF SELECTED COMPONENTS USING A DATABASE EDITOR TOOL	**SECOND SUPPLEMENTAL APPEAL BRIEF**

APPELLANT'S SECOND SUPPLEMENTAL BRIEF
FILED UNDER 37 C.F.R. 1.192

Honorable Commissioner of Patents
and Trademarks
Washington, D.C. 20231

Dear Sir:

CERTIFICATE UNDER 37 C.F.R. 1.8: I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Assistant Commissioner for Patents, Washington, D.C., 20231 on this

30th day of July, 2001.

By John L. Rooney
John L. Rooney

This second supplemental appeal brief is being filed in triplicate within thirty days of and in response to the NOTIFICATION OF NON-COMPLIANCE WITH THE REQUIREMENTS OF 37 CFR

1.192(c) mailed on July 2, 2001. Permission is hereby granted to charge or credit deposit account number 14-0620 for any errors in fee calculation. Appellants request that this Second Supplemental Appeal Brief be made of record and fully considered.

REAL PARTY IN INTEREST

The Real Party in interest is:

Unisys Corporation

Township Line and Union Meeting Roads

Blue Bell, Pennsylvania 19424

being the assignee of the entire right, title, and interest by all inventors, by way of assignment documents filed at Reel 8410, frame 0624, in the United States Patent and Trademark Office.

RELATED APPEALS AND INTERFERENCES

It is Applicants' position that there are no known pending Appeals and/or Interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal. Apparently, the Examiner disagrees. On February 13, 2001, the Examiner mailed Paper No. 9, NOTIFICATION OF NON-COMPLIANCE WITH THE REQUIREMENTS OF 37 CFR 1.192(c), which has required Applicants to supplement their Appeal Brief by stating

that there are pending appeals with regard to the following applications, all filed on January 27, 1997:

U.S. Patent Application Serial No. 08/789,024;

U.S. Patent Application Serial No. 08/789,026;

U.S. Patent Application Serial No. 08/789,027;

U.S. Patent Application Serial No. 08/789,028; and

U.S. Patent Application Serial No. 08/789,029.

TABLE OF CONTENTS

STATUS OF CLAIMS

The subject patent application was filed on January 27, 1997 containing claims 1-41. These claims have all been rejected on three occasions. However, claims 1-41 have not been amended and remain as originally presented.

STATUS OF THE AMENDMENTS

Claims 1-41, being all pending claims, are as originally filed on January 27, 1997. No amendments to the claims have been filed.

SUMMARY OF INVENTION [1]

Applicants' invention, as disclosed and claimed, is a system for and method of efficiently viewing a number of selected components using a database editor tool[2]. Though considerable discussion within the specification relates to the details of the design process, the present invention as disclosed and claimed particularly relates to a method and apparatus for efficiently

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[1] The references to the specification and drawings provided herein are only exemplary and are not deemed to be limiting. The purpose of the references is to enable the Board to more quickly determine where the claimed subject matter is described within the present application.
[2]See title of application.

viewing a selected list of components using a database editor tool[3].

The design process for all integrated circuits is composed of several discrete operations[4]. Initially, the proposed functionality for a circuit is analyzed by one or more chip designers[5]. These designers define the logical components of the circuit and their interactions by specifying the logic design using design capture tools[6]. These design capture tools are commonly implemented in software executing on an engineering workstation, with well-known input devices being used to receive design information from the chip designer, and output devices, such as computer displays, being used to provide visual feedback of the design to the designer as it is being constructed[7].

Chip designers generally employ hierarchical design techniques to determine the appropriate selection and interconnection of logic and/or memory devices which will enable the chip to perform the desired function[8]. These techniques involve describing the chip's functionality at various levels of abstraction, ranging from the

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[3]See page 2, lines 5-7.
[4]See page 2, lines 8-10.
[5]See page 2, lines 10-11.
[6]See page 2, lines 11-14.
[7]See page 2, lines 14-20.
[8]See page 2, line 25, through page 3, line 2.

most general function performed by the chip to the precise functions performed by each logic and/or memory element on the chip[9]. A common method for specifying the integrated circuit design is through the use of hardware description languages[10]. This method allows a circuit designer to specify the circuit at the register transfer level (also known as a "behavior description")[11]. An alternative way of describing the functional integrated circuit design is through a schematic capture tool, which allows the circuit designer to directly enter the schematic for a portion of the circuit design[12].

It is useful to distinguish between those components of an integrated circuit design called cells, provided by a silicon chip vendor as primitive cells (i.e., leaf candidates), and the user-defined hierarchy blocks built upon them[13]. When a given component is specified as part of a given circuit design, it is given an instance name, to distinguish it from all other identical components used in the circuit[14]. As logic blocks are designed and combined, the design becomes a larger design block[15].

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[9]See page 3, lines 2-6.
[10]See page 3, lines 7-8.
[11]See page 3, lines 8-11.
[12]See page 3, lines 22-25.
[13]See page 4, lines 3-7.
[14]See page 4, lines 20-23.
[15]See page 4, line 26, through page 5, line 1.

The generation of the detailed description is often accomplished by logic design synthesis software for HDL entry[16]. This logic design synthesis software generates a gate-level description of the user-defined input and output logic, and also creates new gate-level logic to implement user-defined logical function[17]. Each time the logic design synthesis software is executed for the integrated circuit design, the component and net names which are generated by the software, and not explicitly defined by the user, may change, depending on whether new logic has been added to or deleted from the integrated circuit design[18]. Typically, the logic design synthesis software is executed many times during the integrated circuit design process, because errors may be detected during the simulation and testing phases of the design cycle and then fixed in the behavioral description[19].

The output of the design capture and synthesis tools is a logic design database which completely specifies the logical and functional relationships among the components of the design. Once the design has been converted into this form, it may be optimized by sending the logic design database to a logic optimizer tool

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[16]See page 5, lines 12-14.
[17]See page 5, lines 14-17.
[18]See page 5, lines 20-25.
[19]See page 5, line 25, through page 6, line 4.

implemented in software[20]. Optimization also typically affects the component and net names generated by the logic synthesis tool[21].

After iterative timing verification and functional simulation has been completed on the design, placement and routing of the design's components is performed[22]. These steps involve assigning components of the design to locations on the integrated circuit chip and interconnecting the components to form nets[23]. After the circuit design has been placed and routed, the design is again verified for correctness[24].

Modern integrated circuits often contain tens of thousands of cells[25]. There may be many errors found by the full verification process including both timing related problems and design rule violations. In either case, the circuit design must typically be edited to correct the detected violations. This may require the use of a database editor tool[26]. The detected errors may be logic errors, timing errors, placement errors, or design rule violations[27]. With prior art database editor tools, this correction

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[20]See page 6, lines 5-10.
[21]See page 6, lines 13-15.
[22]See page 7, lines 8-10.
[23]See page 7, lines 10-14.
[24]See page 7, lines 15-16.
[25]See page 8, lines 12-13.
[26]See page 8, lines 13-18.
[27]See page 8, line 20, through page 9, line 3.

process can be tedious and time-consuming because there is not an efficient method for locating the cells or nets involved in the violations[28].

By using a cell selection list that identifies the selected components, the present invention may allow the user to sequentially view the selected components by using a number of pre-defined "hot-keys" (e.g., "V key" or "CTRL-ALT-SHIFT keys")[29]. In addition, the present invention may automatically set the design hierarch in the database editor tool to an appropriate level so that the component being viewed can be easily manipulated by the circuit designer[30].

In an exemplary embodiment, the cell selection list is a listing of a number of selected cells of a circuit design. The cell selection list may be generated in a variety of ways. The database editor tool may then read the cell selection list, and may provide a view frame around the first cell[31]. There are a number of options involving the positioning and contents of the view frame.

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[28]See page 9, lines 9-12.
[29]See page 10, lines 5-10.
[30]See page 10, lines 10-14.
[31]See page 10, lines 15-18.

Having thus provided a concise Summary of the Invention as required by 37 CFR 1.192(c)(5), Applicants present the following Claim Chart in fulfillment of the Examiner's requirements of Paper No. 9, paragraph 2:

Claim	Element	Disclosure
1	a	page 33, lines 12-13, Fig. 4, 178;
1	b	page 37, lines 4-8, Fig. 4, 206;
1	c	page 65, lines 16-19, Fig. 11, 576;
2	-	page 42, lines 6-10, Fig. 5, 120;
3	-	page 69, lines 9-13, Fig. 13, 625;
4	-	page 9, lines 16-18;
5	-	page 30, lines 1-3, Fig. 6;
6	-	page 45, lines 15-18;
7	-	page 28, lines 15-18, Fig. 2;
8	-	page 30, lines 3-4, Fig. 3, 72;
9	-	page 28, lines 10-14, Fig. 2;
10	-	page 6, lines 6-11;
11	-	page 9, lines 11-13;
12	-	page 13, lines 1-8;
13	-	page 13, lines 1-8;
14	-	page 13 lines 1-8;
15	-	page 13, lines 1-8;
16	-	page 13, lines 1-8;
17	a	page 64, lines 18-20;
17	b	page 69, lines 9-13, Fig. 13, 625;
17	c	page 69, lines 9-13, Fig. 13, 627;
18	-	page 69, lines 15-17;
19	-	page 9, lines 16-18;
20	-	page 9, lines 16-18;
21	-	page 30, lines 1-3, Fig. 6;
22	-	page 45, lines 15-18;
23	a	page 64, lines 18-20;
23	b	page 37, lines 4-8, Fig. 4, 206;
23	c	page 69, lines 9-13, Fig. 13, 625;
23	d	page 69, lines 9-13, Fig. 13, 627;
24	a	page 64, lines 18-20;
24	b	page 69, lines 9-13, Fig. 13, 625;
24	c	page 69, lines 9-13, Fig. 13, 629;

25	-	page 45, lines 15-18;
26	-	page 69, lines 9-13, Fig. 13;
27	-	page 69, lines 9-13, Fig. 13;
28	-	page 28, lines 10-14, Fig. 2;
29	-	page 30, lines 1-3, Fig. 6;
30	-	page 9, lines 16-18;
31	-	page 45, lines 15-18;
32	-	page 28, lines 15-18, Fig. 2;
33	-	page 30, lines 3-4, Fig. 3, 72;
34	-	page 28, lines 10-14, Fig. 2;
35	-	page 6, lines 6-11;
36	-	page 9, lines 11-13;
37	-	page 13, lines 1-8;
38	-	page 13, lines 1-8;
39	-	page 13, lines 1-8;
40	-	page 13, lines 1-8; and
41	-	page 13, lines 1-8.

GROUPING OF CLAIMS

Applicants have received three (3) official actions, each rejecting all pending claims (i.e., claims 1-42). In none of these three official actions has the Examiner actually addressed the pending claims individually or even acknowledged that these claims differ in scope from one another. Nevertheless, Applicants deem that pending claims 1-42 are patentably distinct from one another for the reasons provided in the argument below.

ISSUES

1. Is the specification objectionable as failing to properly incorporate essential material?

2. Are claims 1-41 unpatentable for failing to comply with 35 U.S.C. 112, second paragraph?

3. Are claims 1-41 anticipated by each of U.S. Patent No. 5,550,714, issued to Nishiyama; U.S. Patent No. 5,903,466, issued to Beausang et al; U.S. Patent No. 5,581,202, issued to Yano et al; and U.S. Patent No. 5,555,201, issued to Dangelo et al?

GROUPING OF CLAIMS

Applicants have received three (3) official actions, each rejecting all pending claims (i.e., claims 1-41). In none of these three official actions has the Examiner actually addressed the pending claims individually or even acknowledged that these claims differ in scope from one another. Nevertheless, Applicants deem that pending claims 1-41 are patentably distinct from one another for the reasons provided in the argument below.

ARGUMENT

I. The specification is not objectionable for failing to properly incorporate essential material.

At paragraph 3 of Paper No. 6, the Examiner states:

> The attempt to incorporate subject matter into this specification by references to U.S. applications listed on pages 1-2 of the specification is improper because these applications also incorporate essential matter by reference.

The Examiner has conveniently quoted MPEP 608.01(p) which provides in part:

> "Essential material" is defined as that which is necessary to (1) describe the claimed invention, (2) provide an enabling disclosure of the claimed invention, or (3) describe the best mode (35 U.S.C. 112).

Yet, the Examiner has surprisingly not indicated any claim or limitation of any claim which is not supported by the specification as filed, let alone not supported by the combination of the specification and the incorporate materials[32]. Furthermore, the Examiner has failed to indicate why this alleged deficiency was not found in either of the previous two official actions, notwithstanding the prior rejections of all claims on both occasions.

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[32]To fully sustain the rejection, of course, the Examiner would also need to demonstrate that the incorporated U.S. Patent Applications, some having already issued as U.S. Patents , themselves incorporate essential material.

It is Applicants' position that claims 1-41 are fully supported by the specification as filed. However, in the absence of any indication which claims and/or limitations are not completely supported by the subject disclosure, it would be unduly burdensome for Applicants to describe (and for the Board to read) how each and every limitation of all 41 pending claims are completely supported by the current specification.

The pending objection to the specification and any potential rejections based thereon should be reversed as factually incorrect, legally insufficient, and logically inconsistent.

II. Claims 1-41 are not unpatentable for failing to comply with 35 U.S.C. 112, second paragraph.

In paragraph 6, the Examiner has rejected claims 1-41, all pending claims, under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner states in part:

> Examples are provided for Representative. Representative is responsible for locating and correcting all other and similar instances.

The undersigned vehemently disagrees with the Examiner that it is the responsibility of Representative to locate "other and similar

instances". Even though errors may have occurred, as a practical matter, Applicants have not knowingly presented "indefinite" claims for examination. Therefore, Applicants have no basis upon which to amend their claims under 35 USC 112, second paragraph, in response to whatever the Examiner may find but has not indicated to be deemed indefinite. Applicants have drafted their claims to clearly and precisely define their invention.

Perhaps more convincing, MPEP 2171 states in pertinent part:

> Although an essential purpose of the examination process is to determine whether or not the claims define an ntion that is both novel and nonobvious over the prior art, another essential purpose of patent examination is to determine whether or not the claims are precise, clear, correct, and unambiguous. (Emphasis added)

Thus, Applicants' position is that it is the Examiner's responsibility to identify claims which he deems "indefinite", and it is Applicants responsibility to respond appropriately. Therefore, the only alleged rejections under 35 U.S.C. 112, second paragrph, addressed in this appeal are those specifically identified by the Examiner.

II.A. Claim 1 is not indefinite.

Claim 1 has been rejected under 35 U.S.C. 112, second paragraph, as being indefinite[33]. The Examiner alleges that "generating", "selecting", and 'establishing" are indefinite for failure to describe "how?" and "by who (sic)?". These questions could very well be answered within the claim 1. However, to do so would, of necessity, narrow the claim, without rendering it more definite with regard to the requirements of 35 U.S.C. 112, second paragraph. Apparently, the Examiner is confused between rejecting claim 1 as being indefinite and rejecting claim 1 as being too broadly drawn.

To the extent that claim 1 is deemed to read upon the prior art, such additional limitation(s) could be added. The preferred embodiments, of course, provide answers to these questions for those specific implementations. However, Applicant is entitled to claim his invention as broadly as is permitted by the prior art. Absent some compelling prior art reason to further limit claim 1, Applicants decline to do so.

The Examiner also finds "hot keys" to be indefinite. This finding should be reversed as a matter of law. A definition and

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[33]It is important to note that claim 1 (along with claims 2-41) has been rejected twice in previous actions without comment regarding the question of indefiniteness. It seems unlikely that the Examiner would need to examine claim 1 for the third time before determining that it is indefinite.

examples of this term may be found in the specification at page 10, lines 5-10.

The rejection of claim 1 as indefinite should be reversed as either clearly erroneous factually or incorrect as a matter of law.

II.B. Claim 2 is not indefinite.

The Examiner has rejected claim 2 under 35 U.S.C. 112, second paragraph, alleging that "options determine the display" is indefinite for not specifying "what options" and "how do they determine the display". Again, these are questions which may be answered by further limiting claim 2. However, there appears to be no particular reason to further limit the claim. Therefore, the rejection of claim 2 under 35 U.S.C. 112, second paragraph, should be reversed as inappropriate in accordance with the reasoning provided above.

II.C. Claim 12 is not indefinite.

Claim 12 has been rejected under 35 U.S.C. 112, second paragraph, for failing to further limit "physical violations". The Examiner queries, "what kind of physical violations"? The specification describes such violations in a number of places including page 13, lines 2-4. However, as explained above, further

limiting claim 12 by specifying "what kind of physical violations" will not render claim 12 more definite with regard to 35 U.S.C. 112, second paragraph. Therefore, this rejection should be reversed.

II.D. Claim 13 is not indefinite.

The Examiner has rejected claim 13 under 35 U.S.C. 112, second paragraph, questioning "parking lot violations". From the complete disclosure, this is clearly a proper subset of "physical violations". This rejection of claim 13 should be reversed as being indefinite itself.

II.E. Claim 14 is not indefinite.

The Examiner has alleged that "off-grid error" is indefinite. The term is defined within the specification, including at page 11, line 25, through page 12, line 5. This rejection should be reversed as legally inadequate.

II.F. Claim 15 is not indefinite.

The Examiner has alleged that "out-of-context error" of claim 15 is indefinite. The detailed description of this term may be found at page 59, lines 10-23.

This rejection should be reversed as clearly erroneous factually and incorrect as a matter of law.

II.G. Claim 16 is not indefinite.

Claim 16 has been found indefinite for failure to further limit "*identify*". However, this term is not used in claim 16. The term "identifying" is utilized twice. Applicants continue to maintain that further claim limitations are not an appropriate response to an improper rejection under 35 U.S.C. 112, second paragraph. This rejection should be reversed as improper.

III. Claims 1-41 are not anticipated by any of U.S. Patent No. 5,550,714, issued to Nishiyama (hereinafter Nishiyama); U.S. Patent No. 5,903,466, issued to Beausang al (hereinafter Beausang); U.S. Patent No. 5,581,202, issued to Yano et al (hereinafter Yano); and U.S. Patent No. 5,555,201, issued to Dangelo et al (hereinafter Dangelo).

In his second Official Action (i.e., Paper No. 3), the Examiner surprisingly found all 41 pending claims to be anticipated by Nishiyama. He made this finding without the application of the prior art to any particular claim and certainly without addressing any particular element of any claim. His complete rejection stated:

> Claims 1-41 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Nishiyama (U.S. Pat. No. 5,550,714).
> See Figs. 1 and 6 of Nishiyama.

In Applicants' response (i.e., Paper No. 4), it was indicated that the rejection of Paper No. 3 was deemed inadequate in view of the controlling law, because the Examiner did not allege that Nishiyama teaches the elements of pending claims 1-41. At that time Applicants cited as typical of the controlling law:

> It is axiomatic that for prior art to anticipate under §102 it has to meet every element of the claimed invention, and that such a determination is one of fact.

> *Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 231 USPQ 81, 90 (Fed. Cir. 1986).

In response thereto, the Examiner mailed the third Official Action (i.e., Paper No. 6) which additionally finds Beausang, Yano, and Dangelo to anticipate all 41 pending claims and, instead of applying the prior art, simply quotes approximately 14 pages of the various prior art references without substantive comment. Paragraph 16 of Paper No. 6 states:

> As per remarks (page 4, paper #4) concerning the Nishiyama rejection, Representative has provided <u>no substantial evidence showing that Nishiyama does not teach</u> user manipulation of design database elements other that (sic) the reference to fig. 1. (emphasis added)

Thus, it appears that the Examiner places the burden of proof upon Applicants to show non-anticipation, without having first attempting to establish a *prima facie* case of anticipation.

In order to resolve this problem, on the morning of August 17, 2000, a telephonic interview was conducted with the Examiner and his Supervisor, Mr. Kevin Teska. At that time no agreement was reached. However, without citing any particular authority, the Examiner stated that the law presented in the above quoted *Hybritech, Inc. v. Monoclonal Antibodies, Inc.* is no longer controlling. Neither the Examiner nor his Supervisor was able

and/or willing to further define his view of the controlling law of anticipation at that time.

Therefore, certain research was undertaken. The following is a quotation from MPEP 2131, which states in part:

> TO ANTICIPATE A CLAIM, THE REFERENCE MUST TEACH EVERY ELEMENT OF THE CLAIM
>
> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Note that, in some circumstances, it is permissible to use multiple references in a 35 U.S.C. 102 rejection. See MPEP 2131.01. (emphasis added)

Thus, the law seems quite clear. And yet, the Examiner, for whatever reason, inexplicably refuses to apply the controlling law.

The rejection of claims 1-41 as anticipated by the prior art of record should be reversed as incorrect as a matter of law.

III.A. Claim 1 is not anticipated by the prior art of record.

Claim 1 is an independent method claim limited to the combination of three (3) steps: 1) generating a selection list ...;

2) selecting ...; and 3) establishing a view frame .... The Examiner has not alleged that any of the prior art has any of this elements. None of the cited prior art has any of these elements.

This rejection of claim 1 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.B. Claim 2 is not anticipated by the prior art of record.

Claim 2 is a method claim which depends from claim 1. It is further limited by the step of "receiving a number of user defined display options ....". The Examiner does not allege that any of the prior art references teaches this limitation. In fact, none of the prior art of record teaches this limitation. This limitation also renders claim 2 patentably distinct from claim 1.

This rejection of claim 2 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.C. Claim 3 is not anticipated by the prior art of record.

Claim 3 is a method claim which depends from claim 1 and is further limiting of the "establishing" step. This step is not

alleged to be taught in any of the prior art of record and in fact is not found in these references. This limitation renders claim 3 separately patentable over claim 1.

This rejection of claim 3 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.D. Claim 4 is not anticipated by the prior art of record.

Claim 4 is a method claim which depends from claim 1. It is further limited by a "selectively editing ..." step. This limitation is not found in the prior art of record. It renders claim 4 patentable over claim 1.

This rejection of claim 4 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.E. Claims 5 is not anticipated by the prior art of record.

Claim 5 is a method claim which depends from claim 4. It is further limited by a hierarchical database having specific characteristics. This renders claim 5 patentable over claim 4.

This rejection of claim 5 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.F. Claim 6 is not anticipated by the prior art of record.

Claim 6 is a method claim which depends from claim 5. It further limits the "establishing" step with a "setting" step. This renders claim 6 patentable over claim 5.

This rejection of claim 6 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.G. Claim 7 is not anticipated by the prior art of record.

Claim 7 is a method claim which depends from claim 6. It further limits the database to a physical design database. This renders claim 7 patentable over claim 6.

This rejection of claim 7 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.H. Claim 8 is not anticipated by the prior art of record.

Claim 8 is a method claim which depends from claim 7. It further limits the database to a physical placement database. This renders claim 8 patentable over claim 7.

This rejection of claim 8 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.I. Claim 9 is not anticipated by the prior art of record.

Claim 9 is a method claim which depends from claim 1. It further limits the design database to a schematic design database. This renders claim 9 independently patentable over the prior art of record as discussed above and also patentable over claim 8.

This rejection of claim 9 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.J. Claim 10 is not anticipated by the prior art of record.

Claim 10 is a method claim which depends from claim 1. It further limits the database to a simulation design database. This renders claim 10 independently patentable over the prior art of record as discussed above and also patentable over claim 1.

This rejection of claim 10 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.K. Claim 11 is not anticipated by the prior art of record.

Claim 11 is a method claim which depends from claim 1. It further limits the "generating" step to include a "physical violation checking" step. This limitation renders claim 11 patentable over claim 1.

This rejection of claim 11 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.L. Claim 12 is not anticipated by the prior art of record.

Claim 12 is a method claim which depends from claim 11. It further limits the "physical violations checking" step to search for cell overlap. This limitation renders claim 12 patentable over claim 11.

This rejection of claim 12 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.M. Claim 13 is not anticipated by the prior art of record.

Claim 13 is a method claim which depends from claim 11. It further limits the "physical violations checking" step. This limitation renders claim 13 patentable over claim 11.

This rejection of claim 13 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.N. Claim 14 is not anticipated by the prior art of record.

Claim 14 is a method claim which depends from claim 11. It further limits the "physical violations checking" step. This further limitation renders claim 14 patentable over claim 11.

This rejection of claim 14 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.O. Claim 15 is not anticipated by the prior art of record.

Claim 15 is a method claim which depends from claim 11. It further limits the "physical violations checking" step. This further limitation renders claim 15 patentable over claim 11.

This rejection of claim 15 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.P. Claim 16 is not anticipated by the prior art of record.

Claim 16 is a method claim which depends from claim 11. It further limits the "generating" step to include a "timing violation checking" step. This renders claim 16 patentable over claim 11.

This rejection of claim 16 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.Q. Claim 17 is not anticipated by the prior art of record.

Claim 17 is an independent method claim which is distinguishable from claim 1 in that it has two "establishing"

steps rather than one. This further limitation renders claim 17 patentable over claim 1 and the prior art of record.

This rejection of claim 17 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.R. Claim 18 is not anticipated by the prior art of record.

Claim 18 is a method claim which depends from claim 17. It is further limited by repeating step c. This further limitation renders claim 18 patentable over claim 17.

This rejection of claim 18 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.S. Claim 19 is not anticipated by the prior art of record.

Claim 19 is a method claim which depends from claim 17. It is further limited to a "selectively editing" step which renders claim 19 patentable over claim 17.

This rejection of claim 19 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.T. Claim 20 is not anticipated by the prior art of record.

Claim 20 is a method claim which depends from claim 19. It is further limited by a "selectively editing" step. This further limitation renders claim 20 patentable over claim 19.

This rejection of claim 20 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.U. Claim 21 is not anticipated by the prior art of record.

Claim 21 is a method claim which depends from claim 19. It further limits the circuit design database. This further limitation renders claim 21 patentable over claim 19.

This rejection of claim 21 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.V. Claim 22 is not anticipated by the prior art of record.

Claim 22 is a method claim which depends from claim 21. It is further limited by a "setting" step. This further limitation renders claim 22 patentable over claim 21.

This rejection of claim 22 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.W. Claim 23 is not anticipated by the prior art of record.

Claim 23 is an independent method claim which is limited by "generating", "selecting", and two "establishing" steps. These limitations render claim 23 separately patentable over the prior art of record.

This rejection of claim 23 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.X. Claim 24 is not anticipated by the prior art of record.

Claim 24 is an independent apparatus claim which is limited by a "cell selection list", a "viewing means", and a "user control means" . These limitations render claim 24 separately patentable over the prior art of record.

This rejection of claim 24 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.Y. Claim 25 is not anticipated by the prior art of record.

Claim 25 is an apparatus claim which depends from claim 24. It further limits the "viewing means". This further limitation renders claim 25 patentable over claim 24.

This rejection of claim 25 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.Z. Claim 26 is not anticipated by the prior art of record.

Claim 26 is an apparatus claim which depends from claim 24. It further limits the "user control means". This further limitation renders claim 26 patentable over claim 24.

This rejection of claim 26 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.AA. Claim 27 is not anticipated by the prior art of record.

Claim 27 is an apparatus claim which depends from claim 26. It further limits the "hot key" of claim 26. This further limitation renders claim 27 patentable over claim 26.

This rejection of claim 27 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.AB. Claim 28 is not anticipated by the prior art of record.

Claim 28 is an apparatus claim which depends from claim 24. It is further limited by a "circuit design database editor". This limitation renders claim 28 patentable over claim 24.

This rejection of claim 28 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.AC. Claim 29 is not anticipated by the prior art of record.

Claim 29 is an apparatus claim which depends from claim 28. It further limits the "circuit design database". Claim 29 is independently patentable over the prior art and patentable over claim 28 from which it depends.

This rejection of claim 29 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.AD. Claim 30 is not anticipated by the prior art of record.

Claim 30 is an apparatus claim which depends from claim 29. It further limits the "circuit design database editor". Claim 30 is independently patentable over the prior art and patentable over claim 28 from which it depends.

This rejection of claim 30 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.AE. Claim 31 is not anticipated by the prior art of record.

Claim 31 is an apparatus claim which depends from claim 30. It is further limited by a "hierarchy control means". Claim 31 is independently patentable over the prior art and patentable over claim 30 from which it depends.

This rejection of claim 31 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.AF. Claim 32 is not anticipated by the prior art of record.

Claim 32 is an apparatus claim which depends from claim 31. It further limits the circuit design database. Claim 32 is independently patentable over the prior art and patentable over claim 31 from which it depends.

This rejection of claim 32 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.AG. Claim 33 is not anticipated by the prior art of record.

Claim 33 is an apparatus claim which depends from claim 32. It further limits the "physical design database". Claim 33 is

independently patentable over the prior art and patentable over claim 32 from which it depends.

This rejection of claim 33 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.AH. Claim 34 is not anticipated by the prior art of record.

Claim 34 is an apparatus claim which depends from claim 24. It further limits the "circuit design database". Claim 34 is independently patentable over the prior art and patentable over claim 24 from which it depends.

This rejection of claim 34 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.AI. Claim 35 is not anticipated by the prior art of record.

Claim 35 is an apparatus claim which depends from claim 24. It further limits the "circuit design database". Claim 35 is independently patentable over the prior art and claim 24 from which it depends.

This rejection of claim 35 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.AJ. Claim 36 is not anticipated by the prior art of record.

Claim 36 is an apparatus claim which depends from claim 24. It further limits the "cell selection generating means". Claim 36 is independently patentable over the prior art and over claim 24 from which it depends.

This rejection of claim 36 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.AK. Claim 37 is not anticipated by the prior art of record.

Claim 37 is an apparatus claim which depends from claim 36. It further limits the "physical violations checking means". Claim 37 is independently patentable over the prior art and over claim 36 from which it depends.

This rejection of claim 37 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.AL. Claim 38 is not anticipated by the prior art of record.

Claim 38 is an apparatus claim which depends from claim 36. It further limits the "physical violations checking means". Claim 38 is independently patentable over the prior art and over claim 36 from which it depends.

This rejection of claim 38 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.AM. Claim 39 is not anticipated by the prior art of record.

Claim 39 is an apparatus claim which depends from claim 36. It further limits the "physical violations checking means". Claim 39 is independently patentable over the prior art and over claim 36 from which it depends.

This rejection of claim 39 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.AN. Claim 40 is not anticipated by the prior art of record.

Claim 40 is an apparatus claim which depends from claim 36. It further limits the "physical violations checking means". Claim 40 is independently patentable over the prior art and over claim 36 from which it depends.

This rejection of claim 40 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

III.AO. Claim 41 is not anticipated by the prior art of record.

Claim 41 is an apparatus claim which depends from claim 36. It further limits the "cell selection list generating means". Claim 41 is independently patentable over the prior art and over claim 36 from which it depends.

This rejection of claim 41 should be reversed as legally incorrect, procedurally inadequate, and based upon clearly erroneous findings of fact.

CONCLUSION

Having thus reviewed the third non-final rejections of claims 1-41, being all pending claims, it seems abundantly clear that the limitations of these claims are not indefinite and are not unpatentable in view of the prior art of record. Thus, the rejection of these claims should be reversed as being based upon clearly erroneous fact findings and errors of law.

Respectfully submitted

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APPENDIX

1. A method for displaying a number of selected cells on a cathode ray tube, wherein the number of selected cells are represented in a circuit design database, the method comprising the steps of:

a. generating a selection list of the selected cells;

b. selecting at least one of the selected cells; and

c. establishing a view frame around the at least one of the selected cells selected in step (b) by depressing a number of predefined hot keys.

2. A method according to claim 1 further comprising the step of receiving a number of user defined display options, wherein the user defined display options determine the display of the circuit design database in the established view frame.

3. A method according to claim 1 wherein said establishing step sequentially establishes a view frame around selected cells in the selection list when the number of hot key(s) are sequentially depressed.

4. A method according to claim 1 further comprising the step of selectively editing the circuit design database after the view frame is established.

5. A method according to 4 wherein the circuit design database includes a number of levels of hierarchy, and wherein each of the selected cells has a predefined top level of hierarchy that corresponds to one of the number of levels of hierarchy in the circuit design database.

6. A method according to claim 5 wherein said establishing step includes the step of setting the hierarchical level, within a circuit design database editor, to a predetermined level that is at or above the predefined top level of hierarchy of the corresponding cell(s) when said establishing step establishes a view frame therearound.

7. A method according to claim 6 wherein said circuit design database is a physical design database representing a physical design of the circuit design.

8. A method according to claim 7 wherein said physical design database is a placement design database, representing a placement of predefined cells of the circuit design database.

9. A method according to claim 1 wherein said circuit design database is a schematic design database representing a schematic representation of the circuit design.

10. A method according to claim 1 wherein said circuit design database is a simulation design database.

11. A method according to claim 1 wherein said generating step includes a physical violation checking step for identifying a number of physical violations in the circuit design database, and for identifying selected ones of the number of cells that caused selected ones of the number of physical violations.

12. A method according to claim 11 wherein said physical violations checking step checks for cell overlaps.

13. A method according to claim 11 wherein said physical violations checking step checks for parking lot violations.

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14. A method according to claim 11 wherein said physical violations checking step checks for off-grid errors.

15. A method according to claim 11 wherein said physical violations checking step checks for out-of-context cells.

16. A method according to claim 11 wherein said generating step includes a timing violation checking step for identifying a number of timing violations in the circuit design, and for identifying selected ones of the number of cells that should be substituted with logically equivalent cells having a different drive strength to minimize the number of timing violations.

17. A method for sequentially viewing a number of selected cells, wherein the number of selected cells are represented in a circuit design database, the method comprising the steps of:

a. generating a selection list of the selected cells, wherein the selected cells are sequentially ordered in the selection list;

b. establishing a view frame around a first cell selected from the selection list when a predefined combination of hot keys are depressed; and

c. establishing a view frame around a next cell wherein the next cell sequentially follows the first cell in the selection list when the predefined combination of hot keys is again depressed.

18. A method according to claim 17 wherein step (c) is repeated until the remaining cells in the selection list have each had a view frame established therearound.

19. A method according to claim 17 further comprising the step of selectively editing the circuit design database after the view frame has been established around the first cell.

20. A method according to claim 19 further comprising the step of selectively editing the circuit design database after the view frame has been established around the next cell.

21. A method according to claim 19 wherein the circuit design database includes a number of levels of hierarchy, and wherein each of the number of selected cells has a predefined top level of hierarchy that corresponds to one of the number of levels of hierarchy in the circuit design database.

22. A method according to claim 21 further comprising the step of setting the hierarchical level to a predetermined level that is at or above the predefined top level of hierarchy of the first cell when said view frame is established therearound.

23. A method for sequentially viewing a number of selected cells, wherein the number of selected cells are represented in a circuit design database, the method comprising the steps of:

a. generating a selection list of the selected cells, wherein the selected cells are sequentially ordered in the selection list;

b. selecting a first cell from the selection list;

c. establishing a view frame around the first cell when a predefined combination of hot keys are depressed; and

d. establishing a view frame around a next cells wherein the next cell sequentially follows the first cell in the selection list when the predefined combination of hot keys is again depressed.

24. In a data processing system for designing a circuit design, wherein the circuit design is represented in a circuit design database including a number of cells, the improvement comprising:

a. cell selection list generating means for generating a list of selected ones of the number of cells included in the circuit design database;

b. viewing means coupled to said cell selection list generating means for establishing a view frame around at least one of the selected cells; and

c. user control means coupled to said viewing means for allowing a user to control around which of the selected cells that the view frame is established.

25. A data processing system according to claim 24 wherein said viewing means views the circuit design database according to a number of user defined display options.

26. A data processing system according to claim 24 wherein said user control means includes a hot key means, wherein the hot key means establishes the view frame around selected ones of the selected cells each time the hot key means is activated.

27. A data processing system according to claim 26 wherein said hot key mean is activated by depressing a number of predefined hot key(s).

28. A data processing system according to claim 24 further comprising a circuit design database editor for editing the circuit design database.

29. A data processing system according to 28 wherein the circuit design database includes a number of levels of hierarchy, and wherein each of the selected cells has a predefined top level of hierarchy that corresponds to one of the number of levels of hierarchy in the circuit design database.

30. A data processing system according to claim 29 wherein said circuit design database editor allows a user to modify the placement of a selected cell within the circuit design database when the level of hierarchy is set, within the circuit design database editor, to at or above the predefined top level of hierarchy for the selected cell.

31. A data processing system according to claim 30 further comprising a hierarchy control means coupled to said viewing means for setting the hierarchical level, within the circuit design database editor, to a predetermined level that is at or above the predefined top level of hierarchy of the corresponding cell when said viewing means establishes a view frame therearound.

32. A data processing system according to claim 31 wherein said circuit design database is a physical design database representing a physical design of the circuit design.

33. A data processing system according to claim 32 wherein said physical design database is a placement design database, representing a placement of predefined cells of the circuit design database.

34. A data processing system according to claim 24 wherein said circuit design database is a schematic design database representing a schematic representation of the circuit design.

35. A data processing system according to claim 24 wherein said circuit design database is a simulation design database.

36. A data processing system according to claim 24 wherein said cell selection list generating means includes a physical violation checking means for identifying a number of physical violations in the circuit design database, and for identifying selected ones of the number of cells that caused selected ones of the number of physical violations.

37. A data processing system according to claim 36 wherein said physical violations checking means checks for cell overlaps.

38. A data processing system according to claim 36 wherein said physical violations checking means checks for parking lot violations.

39. A data processing system according to claim 36 wherein said physical violations checking means checks for off-grid errors.

40. A data processing system according to claim 36 wherein said physical violations checking means checks for out-of-context cells.

41. A data processing system according to claim 36 wherein said cell selection list generating means includes a timing violation checking means for identifying a number of timing violations in the circuit design, and for identifying selected ones of the number of cells that should be substituted with logically equivalent cells having a different drive strength to minimize the number of timing violations.

METHOD AND APPARATUS FOR EFFICIENTLY VIEWING A NUMBER OF SELECTED COMPONENTS USING A DATABASE EDITOR TOOL

ABSTRACT OF THE DISCLOSURE

A method and apparatus for efficiently viewing selected cells using a database editor tool. By using a cell selection list that identifies a number of selected components, the present invention may allow the user to sequentially view the selected components by using a number of pre-defined "hot-keys". In addition, the present invention may automatically set the design hierarchy in the database editor tool to an appropriate level so that the component being viewed can be easily manipulated by the circuit designer.